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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/495,150	01/31/2000	Gopal Hegde	30019.103US01	4464

7590 01/30/2004

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EXAMINER	
DAY, HERNG DER	

ART UNIT	PAPER NUMBER
2128	12

DATE MAILED: 01/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/495,150	HEGDE ET AL.	
	Examiner	Art Unit	
	Herng-der Day	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2003 and 10 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-12,14,15 and 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-12,14,15 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 January 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This communication is in response to Applicants' Amendment (paper # 9) and RCE (paper # 11) to Office Actions dated August 11, 2003 (paper # 6) and November 3, 2003 (paper # 10), deposited October 13, 2003, and November 7, 2003, respectively.

1-1. Claims 1, 4, 5, 8, 11, 12, 15, and 17 have been amended; claims 6, 13, and 16 have been cancelled; claims 1-5, 7-12, 14-15, and 17 are pending.

1-2. Claims 1-5, 7-12, 14-15, and 17 have been examined and rejected.

Drawings

2. FIG. 5 is objected to for the following reason. A proposed drawing correction or amendment to the specification is required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2-1. For example, as shown in an operation 152 in FIG. 5, "Software CPU Server Invoking Function Calls". However, as shown in FIG. 1, Software 106 is different from CPU Server 112. Therefore, it is unclear what the "Software CPU Server" refers to.

2-2. For example, as shown in an operation 154 in FIG. 5, "Sending A memory Location and/or Value to the Software Server". It is inconsistent with the disclosure of the specification, as described in lines 3-4 of page 18, "an access request from the hardware side is sent to the CPU server at the software side in an operation 154".

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 8-11 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

4-1. For example, the amended claim 8 recites the limitations "hardware component" and "software component" in line 7 of the claim. However, the amended limitations do not appear to be supported by the original specification and it is unclear which component has been referred to. Therefore, claims 8-11 contain subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 7, 14, and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6-1. Claim 7 recites the limitation "receiving test inputs for the co-simulation from a test tool". However, it fails to further limit the subject matter of claim 1 and destroys the limitation recited in claim 1. For the purpose of claim examination, the Examiner will presume that claim

7 recites the limitation "receiving test inputs for the co-simulation from a test tool through the real working environment".

6-2. Claim 14 depends upon the cancelled claim 13. For the purpose of claim examination, the Examiner will presume that claim 14 is a dependent claim of claim 12.

6-3. Claim 17 recites the limitation "the hardware model is configured to receive co-simulation test inputs from a test tool". However, it fails to further limit the subject matter of claim 12 and destroys the limitation recited in claim 12. For the purpose of claim examination, the Examiner will presume that claim 17 recites the limitation "the hardware model is configured to receive co-simulation test inputs from a test tool through the real working environment".

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-5, 7-12, 14-15, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bauer et al., "Hardware/Software Co-Simulation in a VHDL-based Test Bench Approach", Proceedings of the 34th Design Automation Conference, June 1997, pages 774-779, in view of Hollander, U.S. Patent 6,182,258 issued January 30, 2001, and filed February 6, 1998.

8-1. Regarding claim 1, Bauer et al. disclose a method of developing an ASIC comprising:

developing a hardware model including a CPU bus functional model (bus functional model, page 777, section 5.2, paragraph 1) and a software coupled to a CPU server concurrently (software and software server, page 778, section 5.3, paragraphs 4-5);

communicating command and control information between the CPU server and the CPU bus functional model over a network (TCP/IP and FIFO pipe, page 778, section 5.3, paragraphs 7-9);

co-simulating the hardware model and the software (use the unit under test as a hardware model for the software test; software acts as a generator and analyzer for the unit under test, page 774, section 1, paragraph 4).

Bauer et al. fail to expressly disclose receiving real working environment test inputs for the co-simulation.

Hollander discloses a method and apparatus for test generation during circuit design. Specifically, Hollander discloses a co-verification extension module to permit the user to connect to real external data streams (Hollander, column 13, lines 5-8). Hollander also suggests that alternative embodiments can interface with hardware/software co-design environments (Hollander, column 13, lines 12-15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Bauer et al. to incorporate the teachings of Hollander to obtain the invention as specified in claim 1 because Hollander not only discloses using real external data streams as test inputs but also suggests interfacing with hardware/software co-design environments (Hollander, column 13, lines 5-15).

8-2. Regarding claim 2, Bauer et al. further disclose the hardware model is developed on a workstation (same host as the VHDL tool, page 778, section 5.3, paragraph 4).

8-3. Regarding claim 3, Bauer et al. further disclose the software is developed on a target board (test bench, page 778, section 6, paragraphs 2-3).

8-4. Regarding claim 4, Bauer et al. further disclose the network is a TCP/IP protocol network (TCP/IP, page 778, section 5.3, paragraphs 7-8).

8-5. Regarding claim 5, Bauer et al. further disclose the co-simulated hardware model is described by a high-level language model (VHDL simulator, page 778, section 5.3, paragraph 9).

8-6. Regarding claim 7, Bauer et al. further disclose receiving test inputs for the co-simulation from a test tool through the real working environment (Traffic Generator, page 779, Figure 3).

8-7. Regarding claim 8, Bauer et al. disclose a method of co-simulating a hardware model and a software in ASIC development, comprising:

requesting an access to the hardware model including a CPU bus functional model (bus functional model, page 777, section 5.2, paragraph 1) from a hardware side to a software side over a network (software command, page 778, section 5.3, paragraph 6);

invoking a function call by the CPU server (calls the corresponding software routines, page 778, section 5.3, paragraph 6);

sending an access request from the CPU bus functional model to the CPU server over the network (via VHDL communication channels; to TCP/IP link, page 778, section 5.3, paragraph 6);

routing the access request to the hardware model (to the micro processor model, page 778, section 5.3, paragraph 7);

co-simulating the hardware model and the software (use the unit under test as a hardware model for the software test; software acts as a generator and analyzer for the unit under test, page 774, section 1, paragraph 4).

Bauer et al. fail to expressly disclose receiving real working environment test inputs for the co-simulation.

Hollander discloses a method and apparatus for test generation during circuit design. Specifically, Hollander discloses a co-verification extension module to permit the user to connect to real external data streams (Hollander, column 13, lines 5-8). Hollander also suggests that alternative embodiments can interface with hardware/software co-design environments (Hollander, column 13, lines 12-15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Bauer et al. to incorporate the teachings of Hollander to obtain the invention as specified in claim 8 because Hollander not only discloses using real external data streams as test inputs but also suggests interfacing with hardware/software co-design environments (Hollander, column 13, lines 5-15).

8-8. Regarding claim 9, Bauer et al. further disclose the function call is a READ function call (micro processor command; read operation, page 778, section 5.3, paragraph 7).

8-9. Regarding claim 10, Bauer et al. further disclose the function call is a WRITE function call (micro processor command; write operation, page 778, section 5.3, paragraph 7).

8-10. Regarding claim 11, Bauer et al. further disclose comprising:

requesting a hardware model interrupt (an interrupt occurs, page 778, section 5.2, paragraph 4); and

handling the hardware model interrupt with a function call invoked by the software over the network (an exception handling procedure is called, page 778, section 5.2, paragraph 4).

8-11. Regarding claim 12, Bauer et al. disclose an apparatus for hardware model and software co-simulation in ASIC development comprising:

a hardware model including a CPU bus functional model (bus functional model, page 777, section 5.2, paragraph 1) to represent a hardware board circuit (VHDL simulator, page 778, section 5.3, paragraph 9);

a software to provide command and control access of the hardware model (software command, page 778, section 5.3, paragraphs 4-7);

a target board including a CPU server in communication with the software (test bench, page 778, section 6, paragraphs 2-3); and

a network coupled to the CPU bus functional model and the CPU server to communicate a command from the software to the hardware model and to route contents of the command between the hardware model and software, to provide co-simulation of the hardware model and software (TCP/IP and FIFO pipe, page 778, section 5.3, paragraphs 7-9).

Bauer et al. fail to expressly disclose the hardware model is configured to receive real working environment test inputs for the co-simulation.

Hollander discloses a method and apparatus for test generation during circuit design. Specifically, Hollander discloses a co-verification extension module to permit the user to connect to real external data streams (Hollander, column 13, lines 5-8). Hollander also suggests that alternative embodiments can interface with hardware/software co-design environments (Hollander, column 13, lines 12-15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Bauer et al. to incorporate the teachings of Hollander to obtain the invention as specified in claim 12 because Hollander not only discloses using real external data streams as test inputs but also suggests interfacing with hardware/software co-design environments (Hollander, column 13, lines 5-15).

8-12. Regarding claim 14, Bauer et al. further disclose the software is loaded on the CPU server (remote host, page 778, section 5.3, paragraph 4).

8-13. Regarding claim 15, Bauer et al. further disclose the network is a TCP/IP protocol network (TCP/IP, page 778, section 5.3, paragraphs 7-8).

8-14. Regarding claim 17, Bauer et al. further disclose the hardware model is configured to receive co-simulation test inputs from a test tool through the real working environment (Traffic Generator, page 779, Figure 3).

Applicants' Arguments

9. Applicants argue the following:

(1) 35 U.S.C. §132, "Where, as here, the applicants amended only claims, an objection under 35 U.S.C. §132 is improper" (page 8, paper # 9).

(2) 35 U.S.C. §112, first paragraph, "page 18, lines 1-2 of the as-filed specification support the amendment" (page 8, paper # 9).

(3) 35 U.S.C. §112, second paragraph, "the "CPU bus functional model" limitation has sufficient antecedent basis in presently amended independent claim 8" (pages 8-9, paper # 9).

(4) 35 U.S.C. §102(b), "Presently amended independent claim 1 recites in part: ... receiving real working environment test inputs for the co-simulation" and "independent claims 1, 8, and 12 contain a limitation or element not taught by Bauer" (pages 9-10, paper # 9).

(5) 35 U.S.C. §103(a), "Bauer and Rowson individually and in combination fail to teach or suggest all claim limitations in presently amended independent claims 1, 8, and 12" (pages 10-11, paper # 9).

Response to Arguments

10. Applicants' arguments have been fully considered.

10-1. In view of Applicants' persuasive argument (1), the objection to the specification in paper # 6 has been withdrawn.

10-2. In view of Applicants' unpersuasive argument (2), claims 8-11 are rejected under 35 U.S.C. 112, first paragraph, as detailed in section **4-1** above.

10-3. In view of Applicants' persuasive argument (3), the original claim rejections in paper # 6 under 35 U.S.C. 112, second paragraph, for claims 8-11 have been withdrawn after Applicants amended independent claim 8. Claims 7, 14, and 17 are presently rejected under 35 U.S.C. 112, second paragraph, as detailed in sections **6** to **6-1** above.

10-4. In view of Applicants' persuasive arguments (4) and (5), the rejections of claims 1-5, 7-12, 14-15, and 17 under 35 U.S.C. 102(b) and claims 6 and 16 under 35 U.S.C. 103(a) in paper # 6 have been withdrawn after Applicants amended all the independent claims. However, upon further consideration, a new ground of rejection is made, claims 1-5, 7-12, 14-15, and 17 are rejected under 35 U.S.C. 103(a) as detailed in sections **8** to **8-14** above.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Herng-der Day whose telephone number is (703) 305-5269. The examiner can normally be reached on 8:30 - 17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J Teska can be reached on (703) 305-9704. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Herng-der Day
January 25, 2004

HUGH JONES PH.D.
PRIMARY PATENT EXAMINER
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